* Design is 16ft 6in long and 8 feet high\*
* Mass storage 256 bytes, not sorted by data types, only clustered by program
* Ram 64 bytes
  + Ram now reflects actual proportional size
* Code 32 bytes
* Data 16 bytes
* Stack 16 bytes
* Ram can be configured to vary in proportion of memory distribution
* Memory address- base address + offset = address
  + Code segment + IP(PC) = code segment address
  + Data segment + SI/DI = data segment address
  + Stack segment + BP/SP = stack segment address
    - BX can be used in place of a base address
* This diagram includes the control unit
* Op code flows from the code segment of the ram to the IR, before going into the decoder, then the control signal generator.
  + Signal generator sends the appropriate signal to the corresponding components telling them what to do
* No shown connection between signal generator and other components
* This section has a clock to represent the progress of the cycle
* No Queue, will include in next design
* Has AX, BX, CX, DX general purpose registers
* Flags will be displayed on a display, no shown connection to the control unit
* Memory layout is rather set, more unsure of the placement of other groupings
* Unsure of how to group the memory layouts
* Unsure of the offset from the ground, will affect the necessary height for ease of design purposes
* Foam blocks will be readable assembly, broken down into 1 byte segments
* Multi byte instructions will be broken up among different blocks

\*this designs only takes into account the size of the blocks, not any of the necessary sutures which will add size, block displays may need to be further spaced out, this is mainly for what components to have and the rough layout and grouping